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returning the valid copy of the requested data from one of the other processors or memory such that only the processor or memory having the valid copy of the data responds to the request.

9. (Once Amended) A multiprocessor system comprising:

two or more processors, each in communication with a shared memory via a memory controller;

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the processors in communication with the memory controller for issuing a request for data, each of the processors and the shared memory being capable of storing a copy of the requested data, and each copy of the requested data being associated with state indicating whether the copy is valid or invalid,

each of the processors and the shared memory being responsive to a request to check itself for a valid copy of a requested data such that only the processor or the shared memory having the valid copy responds to the request for the requested data.

19. (Once Amended) A multiprocessor system comprising:

two or more processors, each in communication with a shared memory;

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the processors in communication with the shared memory for issuing a request for data, each of the processors and the shared memory being capable of storing a copy of the requested data, and each copy of the requested data being associated with state indicating whether the copy is valid or invalid;

each of the processors and the shared memory being responsive to a request to check itself for a valid copy of a requested data such that only the processor or shared memory having the valid copy responds to the request for the requested data.

Please add the following claims.

21. (Newly added) The method of claim 1, wherein the returning the valid copy of the requested data is asynchronously.

22. (Newly added) The system of claim 9, wherein the processor or the shared memory responding to the request is configured to respond to the request asynchronously.

23. (Newly added) The system of claim 19, wherein the processor or the shared memory responding to the request is configured to respond to the request asynchronously.

TIMELY FILED

The current reply is filed on November 12, 2002, on the first business day following November 11, 2002, which is a federal holiday. Thus, this reply is considered to be timely filed within two months from the date of the Final Office Action.

PENDING CLAIMS

By this reply, claims 1, 9, and 19 have been amended and claims 21-23 have been added. Thus, claims 1-23 are pending.

Claim 1, 9, and 19 have been amended broaden the scope of the claims as well as to correct antecedent basis errors.

35 U.S.C. §103 REJECTION BASED ON CHANG AND WATANABE

In the Final Office Action, claims 1-20 stand rejected under 35 U.S.C. §103(a) as being obvious over Chang et al. USPN 6,119,204 ("Chang") in view of Official Notice taken in the First Office Action dated March 13, 2002 ("First Office Action"). In response to the

Reply to the First Office Action filed on June 13, 2002 ("First Reply") requesting support for the Official Notice, Watanabe USPN 6,067,626 ("Watanabe") was cited in the Final Office Action. Therefore, Applicant will treat the rejection of claims 1-20 as a Section 103 rejection based on Chang and Watanabe. As such, Applicant respectfully traverses.

When making a rejection under 35 U.S.C. § 103, a necessary condition is that the combination of the cited references must teach or suggest all claim limitations. *See M.P.E.P. § 2142.* If the cited references do not teach or suggest every element of the claimed invention, then the cited references fail to render obvious the claimed invention, i.e. the claimed invention is distinguishable over the combination of the cited references.

With respect to independent claims 1, 9, and 19, the combination of Chang and Watanabe fails to teach or suggest every element of these independent claims. Because the combination fails to teach or suggest every element, these claims are not rendered obvious by the combination of Chang and Watanabe.

For example, independent claim 1 recites, *inter alia*, "issuing a request for data to one or more other processors and memory". With reference to Chang, it is stated in the Final Office Action that such is taught as "interconnect 16 includes a broadcast fabric, each device connected to interconnect 16 snoops all communication transactions on interconnect 16" (see first paragraph of item 4 of the Final Office Action). In support of this allegation, Figures 1, 2, and 3 and column 7, lines 35-38 and column 4, lines 23-34 of Chang are cited.

However, "snooping" is clearly not equivalent to "issuing a request". Indeed, Chang does not teach or suggest issuing a request for data at all in the cited portions nor anywhere else. As noted in previous responses to Office Actions, Chang is concerned with whether addresses in the page table entry (PTE) of the table lookaside buffer (TLB) within a processor is valid or not. There is nothing in Chang that teaches or suggests checking whether or not the actual data referenced by the particular address is valid or not.

In the Final Office Action, it appears that the "addresses" in the TLB are equated with data as recited in claim 1. Even with such an interpretation, Chang still does not teach or suggest issuing a request for data as claimed. When a particular processor discovers its TLB is invalid, Chang discloses that particular processor "initiates" a process whereby TLB entries of all processors, including itself, are invalidated and resynchronized (see column 7, line 38 – column 12, line 19 and Figures 4A and 4B of Chang). As shown in Figure 4A of Chang, a processor initiates TLB invalidation process by processing a sequence of instructions TLBIE(s)-SYNC-TLBSYNC-SYNC (see column 7, lines 45-48). As part of executing these sequences of instructions, the initiating processor issues one or more TLBIE instructions on the interconnect 16 (see Figure 4A, blocks 120, 122, and 130 and column 8, lines 54-67) which is then detected by the other processors snooping the interconnect 16. In response to the TLBIE instruction, other processors invalidate their own TLB entries (see Figure 4B).

It is noted that the TLBIE instruction is simply an instruction to perform an action and is NOT an instruction to request data from other processors or from memory. Clearly, TLBIE cannot be equated with a "request" of data. Thus Chang cannot teach or suggest "issuing a request for data" as recited in claim 1. Watanabe has not been cited, and indeed cannot be cited, to cure at least this deficiency of Chang.

It is noted that claim 1 also recites, in part, "in each of the processors and memory that receive the request, checking to determine whether a valid copy of the data exists" and "returning the valid copy of the requested data from one of the other processors or memory such that only the processor or memory having the valid copy of the data responds to the request." Clearly, since Chang does not teach or suggest "request for data", Chang cannot teach or suggest receiving the request nor can it teach or suggest responding to the request. Again, Watanabe has not been cited, and cannot be cited, to cure at least these deficiencies of Chang.

Thus, for at least the reasons stated above, claim 1 is not rendered obvious by the combination of Chang and Watanabe.

Independent claims 9 and 19 recite, in part, "the processors ... issuing a request for data" and "each of the processors and the shared memory being responsive to a request". For reasons similar to stated for independent claim 1, claim 9 and 19 are also not rendered obvious by the combination of Chang and Watanabe.

Claims 2-8, 10-18, and 20 depend from independent claims 1, 9, and 19 directly or indirectly. Therefore, for at least the reasons stated with respect to claims 1, 9, and 19, these dependent claims are also not rendered obvious by the combination of Chang and Watanabe.

Applicant respectfully requests that the rejection of claims 1-20 be withdrawn.

NEW CLAIMS

By this reply, claims 21-23 have been added. These claims depend from independent claims 1, 9, and 19 directly or indirectly. In addition, claim 21 recites, in part, "returning the valid copy of the requested data is asynchronously." Claims 22 and 23 recite a similar feature. It is clear that neither Chang nor Watanabe teaches or suggests at least this feature. For at least the reasons stated above, claims 21-23 are not rendered obvious by the combination of Chang and Watanabe.

Applicant respectfully requests that claims 21-23 be allowed.

CONCLUSION

As all of the outstanding rejections have been traversed and all of the claims are believed to be in condition for allowance, the Applicant respectfully requests issuance of a Notice of Allowability. If the undersigned attorney can assist in any matters regarding

examination of this application, the Examiner is encouraged to call at the number listed below.

Respectfully submitted,

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